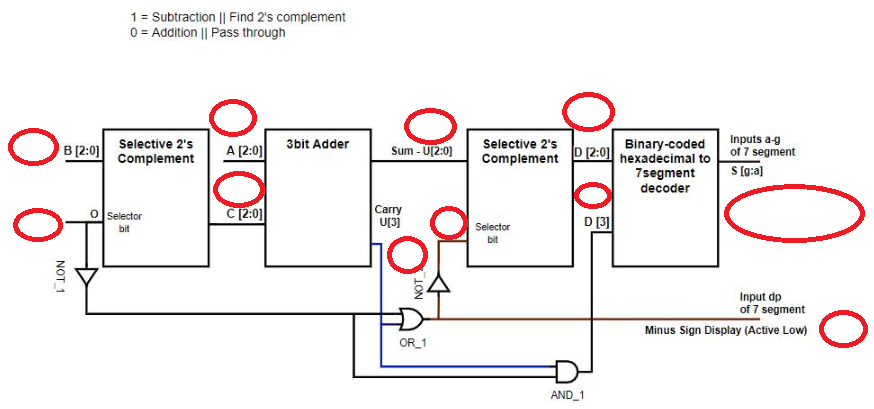
# Lab 06 – Worksheet

|  |  |  |
| --- | --- | --- |
| Name: Ali Muhammad Asad | ID: 07190 | Section: T6 |

## Introduction

Label the figure below *or* type test cases which you have performed on given design during the lab:



|  |
| --- |
|  |

1. **7-Segment Hexadecimal Display Decoder**

Table 6.1

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Hex Digit** | **Binary-coded Hexadecimal/ Inputs to decoder** | | | | **Outputs of the decoder** | | | | | | |
| **D3** | **D2** | **D1** | **D0** | **Sg** | **Sf** | **Se** | **Sd** | **Sc** | **Sb** | **Sa** |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 2 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 4 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 5 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| A | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| B | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| C | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| D | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| E | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| F | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

Write Boolean expression for each output segment.

Table 6.2

|  |  |
| --- | --- |
| Sa = | D3’D2’D1’D0 + D3’D2D1’D0’ + D3D2’D1D0 + D3D2D1’D0 |
| Sb = | D3’D2D1’D0 + D3D1D0 + D3D2D0’ + D2D1D0’ |
| Sc = | D3’D2’D1D0’ + D3D2D0’ + D3D2D1 |
| Sd = | D3’D2’D1’D0 + D3’D2D1’D0’ + D2D1D0 + D3D2’D1D0’ |
| Se = | D3’D0 + D3’D2D1’ + D2’D1’D0 |
| Sf = | D3’D2’D0 + D3’D2’D1 + D3’D1D0 + D3D2D1’D0 |
| Sg = | D3’D2’D1’ + D3’D2D1D0 + D3D2D1’D0’ |

*Appropriately add comments to your code and* ***write*** *the code of your design module in the box below.*

|  |
| --- |
| `timescale 1ns / 1ps  module seven\_segment(  input [3:0] D,  output [6:0] S  );  //Write your code here  assign S[0] = (~D[3]&~D[2]&~D[1]&D[0]) | (~D[3]&D[2]&~D[1]&~D[0]) | (D[3]&~D[2]&D[1]&D[0]) | (D[3]&D[2]&~D[1]&D[0]);  assign S[1] = (D[2]&D[1]&~D[0]) | (D[3]&D[1]&D[0]) | (D[3]&D[2]&~D[0]) | (~D[3]&D[2]&~D[1]&D[0]);  assign S[2] = (D[3]&D[2]&~D[0]) | (D[3]&D[2]&D[1]) | (~D[3]&~D[2]&D[1]&~D[0]);  assign S[3] = (D[2]&D[1]&D[0]) | (~D[3]&~D[2]&~D[1]&D[0]) | (~D[3]&D[2]&~D[1]&~D[0]) | (D[3]&~D[2]&D[1]&~D[0]);  assign S[4] = (~D[3]&D[0]) | (~D[2]&~D[1]&D[0]) | (~D[3]&D[2]&~D[1]);  assign S[5] = (~D[3]&~D[2]&D[0]) | (~D[3]&~D[2]&D[1]) | (~D[3]&D[1]&D[0]) | (D[3]&D[2]&~D[1]&D[0]);  assign S[6] = (~D[3]&~D[2]&~D[1]) | (~D[3]&D[2]&D[1]&D[0]) | (D[3]&D[2]&~D[1]&~D[0]);  endmodule |

*Attach RTL Schematic of the module.*

|  |
| --- |
|  |

*Attach screenshot of your simulation output window*: (Invert background color to white using settings option in simulation window)

|  |
| --- |
|  |

*Attach screenshot of log-window here*

|  |
| --- |
|  |

## Adder/Subtractor system

*Provide code for design module here*

|  |
| --- |
| `timescale 1ns / 1ps  module threeBitAdder(  input [2:0] A,  input [2:0] B,  output [2:0] Y,  output Cout  );  wire res1, res2;  fulladder t1(A[0], B[0], 0, Y[0], res1);  fulladder t2(A[1], B[1], res1, Y[1], res2);  fulladder t3(A[2], B[2], res2, Y[2], Cout);    endmodule |

*Add your testbench here*

|  |
| --- |
| *module testbench\_threeBitAdder();*  *reg[2:0] aA;*  *reg[2:0] bB;*  *wire [2:0] yY; wire cCout;*  *threeBitAdder test(aA, bB, yY, cCout);*  *initial begin*  *#100 aA =3'b 110 ; bB = 3'b 010; //8*  *#100 aA =3'b 101 ; bB = 3'b 011; //8*  *#100 aA =3'b 100 ; bB = 3'b 110; //10*  *#100 aA =3'b 111 ; bB = 3'b 101; //12*  *#100 aA =3'b 010 ; bB = 3'b 100; //6*  *#100 aA =3'b 011 ; bB = 3'b 001; //4*  *end*  *endmodule* |

*Attach screenshot of waveform results here* (Invert background color to white using settings option in simulation window)

|  |
| --- |
|  |

*Attach screenshot of log-window here*

|  |
| --- |
|  |

## Assessment Rubrics

**Marks Distribution:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | **LR2**  **Code** | **LR4**  **Data**  **Collection** | **LR5**  **Results** | **LR7**  **Viva** | **LR9**  **Report** |
| **In-lab** | **Task a** |  |  |  | 10 points | 10 points |
| **Task b** | 15 points | 20 points | 15 points |  |
| **Task c** | 20 points |  | 10 points |  |
| **Total Marks =** |  | 100 points | | | | |

**Marks Obtained:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | **LR2**  **Code** | **LR4**  **Data**  **Collection** | **LR5**  **Results** | **LR7**  **Viva** | **LR9**  **Report** |
| **In-lab** | **Task a** | - | - | - |  |  |
| **Task b** |  |  |  | - |
| **Task c** |  | - |  | - |
| **Total Marks =** |  |  | | | | |